OIPE JC183
MAR 1 7 2005
PATENT & TRADEMARK OFFICE

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on the below date:

Date: March 14, 2005 Name: Joseph W. Flerlage Signature: JWF

BRINKS HOFER GILSON &LIONE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Appln. of: Hans-Joachim Barth et al.

Appln. No.: 10/518,880

Filed: December 20, 2004

For: LAYER ASSEMBLY AND METHOD FOR PRODUCING A LAYER ASSEMBLY

Attorney Docket No: 10808/158

Examiner:

Art Unit:

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL

Sir:

Attached is/are:

☒ Transmittal letter (in duplicate); Supplemental Information Disclosure Statement; Form PTO-1449; Copy of cited references

☒ Return Receipt Postcard

Fee calculation:

☒ No additional fee is required.

☐ Small Entity.

☐ An extension fee in an amount of $_____ for a _____-month extension of time under 37 C.F.R. § 1.136(a).

☐ A petition or processing fee in an amount of $_____ under 37 C.F.R. § 1.17(_____).

☐ An additional filing fee has been calculated as shown below:

	Claims Remaining After Amendment		Highest No. Previously Paid For	Present Extra		Small Entity Rate	Small Entity Add'l Fee	or	Not a Small Entity Rate	Not a Small Entity Add'l Fee
Total		Minus				x $25=			x $50=	
Indep.		Minus				x 100=			x $200=	
First Presentation of Multiple Dep. Claim						+$180=			+ $360=	
						Total	$		Total	$

Fee payment:

☐ A check in the amount of $_____ is enclosed.

☐ Please charge Deposit Account No. 23-1925 in the amount of $. A copy of this Transmittal is enclosed for this purpose.

☐ Payment by credit card in the amount of $_____ (Form PTO-2038 is attached).

☒ The Director is hereby authorized to charge payment of any additional filing fees required under 37 CFR § 1.16 and any patent application processing fees under 37 CFR § 1.17 associated with this paper (including any extension fee required to ensure that this paper is timely filed), or to credit any overpayment, to Deposit Account No. 23-1925.

Respectfully submitted,

March 14, 2005
Date

JWF
Joseph W. Flerlage (Reg. No. 52,897)

OIPE JC163
MAR 17 2005
PATENT & TRADEMARK OFFICE

DT08 Rec'd PCT/PTO 17 MAR 2005 PCT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Appln. of:	Hans-Joachim Barth et al.		
Appln. No.:	10/518,880	Examiner:	
Filed:	December 20, 2004	Art Unit:	
For:	LAYER ASSEMBLY AND METHOD FOR PRODUCING A LAYER ASSEMBLY		
Attorney Docket No:	10808/158		

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

In accordance with the duty of disclosure under 37 C.F.R. §1.56 and §§1.97-1.98, and more particularly in accordance with 37 C.F.R. §1.97(b), Applicants hereby cite the following reference(s):

No.	Date of Publication	Patentee/Applicant/Assignee
5,882,963	03/16/99	Kerber et al.
6,342,722	01/29/2002	Armacost et al.

FOREIGN PATENT DOCUMENTS

DOCUMENT NUMBER	DATE	COUNTRY
WO 02/19420 A2	03/07/2003	Germany
DE 44 41 898 C1	11/24/2004	PCT

OTHER ART – NON PATENT LITERATURE DOCUMENTS
B.P. Shieh, eth al., "Integration and Reliability Issues for Low Capacitance Air-Gap Interconnect Structures", IEEE, IITC, 1998, pp., 125-127.
O.Demolliens, et al., "Copper-SiOC-AirGap Integration in a Double Level Metal interconnect", Proceedings IITC, 2000, pp. 267, 277.
Dhananjay M. Bhusari et al., "Fabrication of Air-Gaps Between Cu Interconnects for Low Intralevel k", Materials Research Society Symposium Proceedings, Materials Research Society, Pittsburg, PA, US., Vol. 612, April 23, 2000, pp. D4801-D4806.
Paul A. Kohl, et al., "Air-Gaps in 0.3 μm Electrical Interconnections", 2000 IEEE Electron Device Letters, Vol. 21, No. 12, December 2000, pp. 557-559.

Applicants are enclosing Form PTO-1449 (one sheet), along with a copy of each listed reference for which a copy is required under 37 C.F.R. §1.98(a)(2). The German

BRINKS HOFER GILSON &LIONE

Reference DE 44 41 898 C1 relates to manufacturing a semiconductor component where capacitances are reduced by filling cavities with air or gas. A corresponding U.S. Patent No. 5,882,963 is also herein submitted. Applicants respectfully request the Examiner's consideration of the above reference(s) and entry thereof into the record of this application.

By submitting this Statement, Applicants are attempting to fully comply with the duty of candor and good faith mandated by 37 C.F.R. §1.56. As such, this Statement is not intended to constitute an admission that any of the enclosed references, or other information referred to therein, constitutes "prior art" or is otherwise "material to patentability," as that phrase is defined in 37 C.F.R. §1.56(a).

Applicants have calculated no fee to be due in connection with the filing of this Statement. However, the Director is authorized to charge any fee deficiency associated with the filing of this Statement to a deposit account, as authorized in the Transmittal accompanying this Statement.

Respectfully submitted,

March 14, 2005
Date

Joseph W. Flerlage (Reg. No.52,897)

FORM PTO-1449	SERIAL NO. 10/518,880	CASE NO. 10808/158
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	FILING DATE December 20, 2004	GROUP ART UNIT
(use several sheets if necessary)	APPLICANT(S): Hans-Joachim Barth et al.	

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER Number-Kind Code (If known)	DATE	NAME	CLASS/ SUBCLASS	FILING DATE
	A1	5,882,963	03/16/99	Kerber et al.		
	A2	6,342,722	01/29/2002	Armacost et al.		

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER Number-Kind Code (If known)	DATE	COUNTRY	CLASS/ SUBCLASS	TRANSLATION YES OR NO
	A3	WO 02/19420 A2	03/07/2003	Germany		
	A4	DE 44 41 898 C1	11/24/2004	PCT		Yes – See U.S. Patent No. 5,882,963 (above)

EXAMINER INITIAL		**OTHER ART – NON PATENT LITERATURE DOCUMENTS** (Include name of author, title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date page(s), volume-issue number(s), publisher, city and/or country where published.
	A5	B.P. Shieh, eth al., "Integration and Reliability Issues for Low Capacitance Air-Gap Interconnect Structures", IEEE, IITC, 1998, pp., 125-127.
	A6	O.Demolliens, et al., "Copper-SiOC-AirGap Integration in a Double Level Metal interconnect", Proceedings IITC, 2000, pp. 267, 277.
	A7	Dhananjay M. Bhusari et al., "Fabrication of Air-Gaps Between Cu Interconnects for Low Intralevel k", Materials Research Society Symposium Proceedings, Materials Research Society, Pittsburg, PA, US., Vol. 612, April 23, 2000, pp. D4801-D4806.
	A8	Paul A. Kohl, et al., "Air-Gaps in 0.3 μm Electrical Interconnections", 2000 IEEE Electron Device Letters, Vol. 21, No. 12, December 2000, pp. 557-559.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.